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Novel Space Vector Pulse Width Modulation Strategies for Single-Phase Three-Level NPC Impedance-Source Inverters

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***Abstract*— This paper presents new Space Vector Pulse-Width Modulation (SVPWM) strategies for a single-phase three-level buck-boost Neutral Point Clamped (NPC) inverter coupled with Impedance-Source (IS) networks. These strategies can be implemented for systems with any IS networks with neutral point. The case study system is based on the quasi-Z-source inverter with continuous input current. To demonstrate an improved performance, the strategies are compared with a traditional pulse-width modulation strategy. The advantages lie in reduced switching number, without output voltage quality distortion. The simulation and experimental results confirm the theoretical predictions.**

I. Introduction

Present technologies and innovations have led to the expansion of Photovoltaic (PV) energy generation systems worldwide [1]-[4]. PV energy sources are characterized by a wide output voltage and power variation. The solar irradiation level changes significantly during the day and gives a variable output power. Also, the shading or high operating temperature of the PV module leads to a significant out-voltage drop. Therefore, the converter for a PV system should have a wide input voltage and output load regulation range.

To extend the input voltage regulation range, solutions based on Impedance-Source (IS) networks have been proposed [5]-[11]. They have a buck mode, a boost mode and do not suffer from the Shoot-Through (ST) [5] states compare to the conventional grid-connected inverters.

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At the same time, inverters used for PV system integration to the grid can be based on two-level or multilevel topologies. Multilevel inverters are preferable solutions not only for medium-voltage but also for low-voltage applications. One of the most important benefits of the multilevel inverter is reduced voltage stress on the semiconductors. At the same time, the increased number of the output voltage levels leads to an output voltage quality improvement. The Three-Level (3L) Neutral Point Clamped (NPC) inverter is one of the most popular solutions among the multilevel topologies [12]-[18]. In case of full-bridge utilization it gives five-level output voltage.

The latest research [19]-[21] show that any IS networks are feasible for low power application with a wide range input voltage regulation. In most applications, low power facilities are associated with single-phase systems. The latest research [19]-[21] show that any IS networks are feasible for low power application with a wide range input voltage regulation. In most applications, low power facilities are associated with single-phase systems.

Low power applications make such topologies feasible by means of a very high switching frequency that, in turn, reduces the size and weight of the passive components. Switching losses can be reduced by means of novel wide bandgap semiconductors and also different modulation techniques.

There are many well-known Pulse-Width Modulation (PWM) techniques that can be applied for IS based converters [22]-[31]. Space Vector PWM (SVPWM) is mostly applied to three-phase systems [32]-[39]. It can be applied for IS based converters as well [40]-[43].

At the same time, several papers report that SVPWM is suitable for conventional single-phase systems [44]-[47]. Additionally, this technique is effective for use with a voltage unbalancing problem [44]. This technique is proposed only for conventional single-phase three-level inverters. Focus in this work is on the development of a SVPWM for the single-phase 3L NPC buck-boost inverter coupled with any IS network. SVPWM makes the neutral point balancing flexible, improves the output voltage quality, and reduces also the switching losses.

II. Existing SVPWM Techniques for Single-Phase Three-Level Inverter

The 3L NPC buck-boost inverter coupled with IS (quasi-Z-source) network is shown in Fig. 1, where points -1, 0, 1, A, and B are denoted. The 3L quasi-Z-Source NPC inverter is selected as a case study solution [15].

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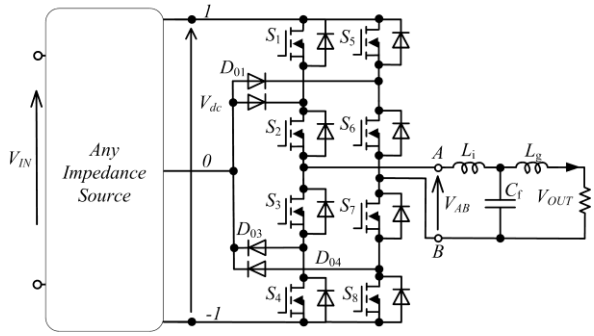

Fig. 1. Single-Phase 3L NPC inverter coupled with IS networks.

Nine switching states are possible for a conventional 3L NPC converter: (-1,-1), (0,0), (1,1), (-1,0), (0,1), (1,-1), (0,-1), (-1,1), and (1,-1), that are illustrated in Table I. Where 1 is denoted as conducting switches S_1-S_8.

TABLE I. SWITCHING STATES FOR A SINGLE-PHASE NPC

State	S 1	S 2	S 3	S 4	S 5	S 6	S 7	S 8	Voltage level V_{AB}	Vectors (Fig. 2*a*)	Vectors (Fig. 2*b*)
-1,-1	0	0	1	1	0	0	1	1	0	V_0	V_0
0,0	0	1	1	0	0	1	1	0	0		
1,1	1	1	0	0	1	1	0	0	0		
1,0	1	1	0	0	0	1	1	0	$V_{dc}/2$	V_4	V_1
0,-1	0	1	1	0	0	0	1	1	$V_{dc}/2$	V_2	
1,-1	1	1	0	0	0	0	1	1	V_{dc}	V_3	V_2
0,1	0	0	1	1	1	1	0	0	$-V_{dc}/2$	V_1	V_3
-1,0	0	0	1	1	0	1	1	0	$-V_{dc}/2$	V_5	
-1,1	0	0	1	1	1	1	0	0	$-V_{dc}$	V_6	V_4

Using these switching states, two space voltage vector diagrams can be shown [45] for a single-phase 3L NPC inverter (Fig. 2).

Fig. 2*a* represents a reference vector V^* synthesized by six non-zero voltage vectors V_1-V_6 and one zero voltage vector V_0. In each of the six sectors (*I*-*VI*) three closer located vectors are used V_j, V_{j+1} and V_0, for synthesizing the reference vector V^*, where j is a vector number. In sector *VI*, the reference vector V^* is synthesized by V_1, V_6 and V_0. The use of V_0 is necessary in order to provide the modulation index in a range of $0 \le M \le 1$.

A weighting coefficient τ_{ij} will be used for the following analysis, where i is the sector number. The weighting coefficient τ_{ij} is the relative duration of the vector V_j during the switching period in sector i. For any sector in Fig. 2a, the weighting coefficients τ can be defined from:

$$\begin{cases} \tau_0 = 1 - \dfrac{M}{\sqrt{3}} \cdot \left(\cos(\vartheta) + \dfrac{1}{\sqrt{3}} \sin(\vartheta) \right) \\ \tau_{i,j} = \dfrac{M}{\sqrt{3}} \cdot \left(\cos(\vartheta) - \dfrac{1}{\sqrt{3}} \sin(\vartheta) \right) \\ \tau_{i,(j+1)} = \dfrac{2}{3} \cdot M \cdot \sin(\vartheta) \\ \tau_{i,j} + \tau_{i,(j+1)} + \tau_0 = 1, \tau_{i,j} = \dfrac{T_{i,j}}{T}, 0° < \vartheta \le 60° \end{cases}, \quad (1)$$

where $T_{i,j}$ is the time interval of the space vector application, T is the switching period.

In the SVPWM shown in Fig. 2*b*, the reference vector V^* is synthesized by four non-zero voltage vectors V_1-V_4 and one zero voltage vector V_0. In each of the eight sectors (*I*-*VIII*) for synthesizing the reference vector V^*, two closer located vectors are used. For example, V_1 and V_0 are used in sector *I*, and V_4 and V_3 in sector *VII*. The weighting coefficients for this approach are given in Table II, where phase ϑ is varying in a range $0° < \vartheta \le 360°$ and S is the number of the sectors.

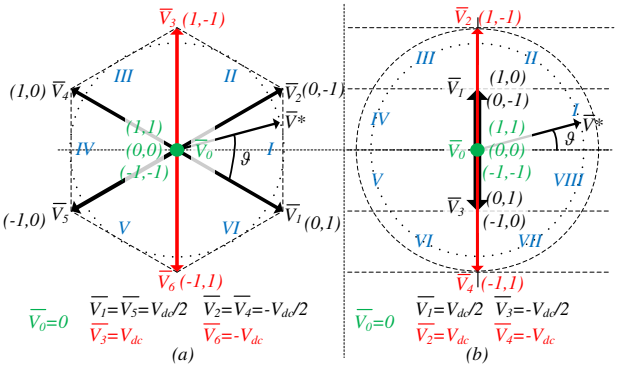

Fig. 2. Space voltage vector diagrams for a single-phase 3L NPC inverter derived by different set of vectors (*a* and *b*).

TABLE II. WEIGHTING COEFFICIENTS FOR SVPWM IN DIFFERENT SECTORS (FIG. 2B)

Sector	Weighting coefficients (τ_{ij})
I, IV	$\begin{cases} \tau_{1,0} = \tau_{4,0} = 1 - 2M\sin(\vartheta) \\ \tau_{1,1} = \tau_{4,1} = 2M\sin(\vartheta) \end{cases}$
II, III	$\begin{cases} \tau_{2,1} = \tau_{3,1} = 2 - 2M\sin(\vartheta) \\ \tau_{2,2} = \tau_{3,2} = 2M\sin(\vartheta) - 1 \end{cases}$
V, VIII	$\begin{cases} \tau_{5,0} = \tau_{8,0} = 1 + 2M\sin(\vartheta) \\ \tau_{5,3} = \tau_{8,3} = -2M\sin(\vartheta) \end{cases}$
VI, VII	$\begin{cases} \tau_{6,3} = \tau_{7,3} = 2 + 2M\sin(\vartheta) \\ \tau_{6,4} = \tau_{7,4} = -1 - 2M\sin(\vartheta) \end{cases}$

In a general case, the weighting coefficients for any SVPWM are calculated according to the principle proposed in [44]. The SVPWM shown in Fig. 2*b* has several key advantages over the SVPWM shown in Fig. 2*a*. First of all, it has 15% larger fundamental harmonic component. Also, the calculation of the weighting coefficients is much easier. Therefore, the SVPWM is shown in Fig. 2*b* will be considered like a basic solution.

III. SVPWM FOR SINGLE-PHASE IS-BASED INVERTER

Fig. 3 shows a proposed space vector diagram for an IS-based Single-Phase 3L NPC inverter along with an example of the switching states distribution in each sector. The main goal of this approach lies in the generation of the optimal switching sequence in terms of minimum switching losses providing the output sinusoidal voltage. At the same time, it should be noted that only equally distributed ST generation is considered. Maximum boost control [22] may evoke oscillation in the IS network and is not feasible for practical implementation. This phenomenon has been shown and discussed in [48].

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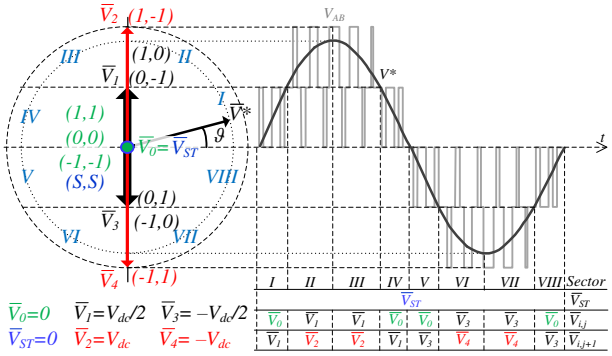

Fig. 3. Space voltage vector diagram for proposed SVPW for single-phase 3L NPC IS inverter.

The vector diagram is divided into eight sectors. It is different by additional ST vector V_{ST}, which is in a response for ST state generation. However, here in each sector, three weighting coefficients must be defined: two for general (closer located) vectors and one for the vector V_{ST}. The vector V_{ST} is used in each sector in order to achieve equally distributed ST generation. The weighting coefficient of V_{ST} is equal to ST duty cycle D_{ST}, determined by capacitor voltage regulator. Taking into account equally distributed ST states (τ_{ST}=const) the weighting coefficients are defined as:

$$\begin{cases} \tau_{ST} = D_S = T_{ST}/T = const, M \le 1 \\ \tau_{ST} + \tau_{i,j} + \tau_{i,(j+1)} = 1 \\ \tau_{i,j} = \dfrac{(1-\tau_{ST})\cdot \vec{V}_{j+1} - \vec{V}^*}{\vec{V}_{j+1} - \vec{V}_j} \\ \tau_{i,(j+1)} = \dfrac{(1-\tau_{ST})\cdot \vec{V}_j - \vec{V}^*}{\vec{V}_j - \vec{V}_{j+1}} \end{cases}, \quad (2)$$

where V_j, V_{j+1} are the space vectors used in sector i and $V^*=(1-\tau_{ST})\cdot M\cdot V_{dc}\sin(\vartheta)$ is the reference vector.

For example, in the sector VII, the output voltage is generated by vectors $\vec{V}_j = \vec{V}_3 = -V_{dc}/2$ and $\vec{V}_{j+1} = \vec{V}_4 = -V_{dc}$. The weighting coefficients are expressed from (2) as:

$$\begin{cases} \tau_{i,j+1} = \tau_{7,4} = \dfrac{(1-\tau_{ST})(\frac{-V_{dc}}{2}) - (1-\tau_{ST})M\cdot V_{dc}\sin\vartheta}{-\frac{V_{dc}}{2} - (-V_{dc})} \\ \tau_{i,j} = \tau_{7,3} = \dfrac{(1-\tau_{ST})(-V_{dc}) - (1-\tau_{ST})M\cdot V_{dc}\sin\vartheta}{-V_{dc} - (-\frac{V_{dc}}{2})} \end{cases}, (3)$$

$$\begin{cases} \tau_{7,4} = \tau_{ST} - 1 - 2\cdot V_Y^* \\ \tau_{7,3} = (1-\tau_{ST})\cdot 2 + 2\cdot V_Y^* \end{cases}, \quad (4)$$

$$V_Y^* = (1-\tau_{ST})\cdot M\cdot \sin\vartheta. \quad (5)$$

Here (5) V^*_Y is y axis projection of V^* in relative units. The calculated weighting coefficients for all sectors are shown in Table III. The vector V^* position and sector boundaries are detected by calculating the rotation angle ϑ value.

One of the very important issues during generation of the sequence of the vector is balancing of the energy utilization from capacitors. It consists in the equal charging and discharging of the different capacitors of IS network. Fig. 4 shows two equivalent switching states of the vector V_1 which generates the voltage equal to $V_{dc}/2$.

In the first case (Fig. 4*a*) the charging current of capacitor C_2 ($i_{C2}=i_{IN}$) is larger than the charging current of capacitor C_3 ($i_{C3}=i_{IN}-i_{dc}$) and vice-versa in the second case (Fig. 4*b*). The principle of the balancing consists in equal utilization of the equivalent circuits shown in Fig. 4 maintaining constant voltage across the capacitors.

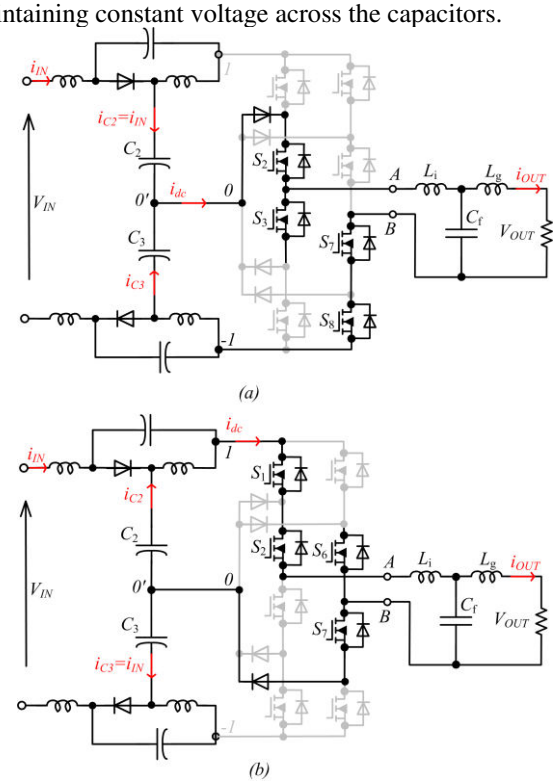

Fig. 4.Equivalent circuits of active states of the quasi-Z-Source NPC inverter.

TABLE III. WEIGHTING COEFFICIENTS OF SVPWM FOR IS INVERTER (FIG. 3)

Weighting coefficients (τ_{ij})	Sector boundaries	
$\begin{cases}\tau_{1,0}=\tau_{40,}=1-\tau_{ST}-2\cdot V_Y^* \\ \tau_{1,1}=\tau_{4,1}=2\cdot V_Y^*\end{cases}$	$I: 0 \le \vartheta < \arcsin\left(\frac{0.5}{M}\right)$	$IV: \pi - \arcsin\left(\frac{0.5}{M}\right) \le \vartheta < \pi$
$\begin{cases}\tau_{2,1}=\tau_{3,1}=(1-\tau_{ST})\cdot 2-2\cdot V_Y^* \\ \tau_{2,2}=\tau_{3,2}=-(1-\tau_{ST})+2\cdot V_Y^*\end{cases}$	$II: \arcsin\left(\frac{0.5}{M}\right) \le \vartheta < \frac{\pi}{2}$	$III: \frac{\pi}{2} \le \vartheta < \pi - \arcsin\left(\frac{0.5}{M}\right)$
$\begin{cases}\tau_{5,0}=\tau_{8,0}=1-\tau_{ST}+2\cdot V_Y^* \\ \tau_{5,3}=\tau_{8,3}=-2\cdot V_Y^*\end{cases}$	$V: \pi \le \vartheta < \pi + \arcsin\left(\frac{0.5}{M}\right)$	$VIII: 2\pi - \arcsin\left(\frac{0.5}{M}\right) \le \vartheta < 2\pi$
$\begin{cases}\tau_{6,3}=\tau_{7,3}=2\cdot(1-\tau_{ST})+2\cdot V_Y^* \\ \tau_{6,4}=\tau_{7,4}=-(1-\tau_{ST})-2\cdot V_Y^*\end{cases}$	$VI: \pi + \arcsin\left(\frac{0.5}{M}\right) \le \vartheta < \frac{3\pi}{2}$	$VII: \frac{3\pi}{2} \le \vartheta < 2\pi - \arcsin\left(\frac{0.5}{M}\right)$

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Sect.	I					II					III					IV					V					VI					VII					VIII				
Vec.	V_{ST}	V_1	V_0	V_1	V_{ST}	V_{ST}	V_1	V_2	V_1	V_{ST}	V_{ST}	V_1	V_2	V_1	V_{ST}	V_{ST}	V_1	V_0	V_1	V_{ST}	V_{ST}	V_3	V_0	V_3	V_{ST}	V_{ST}	V_3	V_4	V_3	V_{ST}	V_{ST}	V_3	V_4	V_3	V_{ST}	V_{ST}	V_3	V_0	V_3	V_{ST}
SS	ST	0,-1	0,0	1,0	ST	ST	0,-1	1,-1	1,0	ST	ST	1,0	1,-1	0,-1	ST	ST	1,0	0,0	0,-1	ST	ST	0,1	0,0	-1,0	ST	ST	0,1	-1,1	-1,0	ST	ST	-1,0	1,-1	0,1	ST	ST	-1,0	0,0	0,1	ST
S_1	1				1	1				1	1	1			1	1				1	1				1	1				1	1				1	1				1
S_2	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1		1	1	1			1	1				1	1		1	1	1
S_3	1	1	1		1	1	1			1	1			1	1	1		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
S_4	1				1	1				1	1				1	1				1	1			1	1	1	1	1	1	1	1	1	1	1	1	1			1
S_5	1				1	1				1	1				1	1				1	1			1	1	1	1	1	1	1			1	1				1	1
S_6	1		1	1	1	1			1	1	1	1			1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
S_7	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1		1	1	1	1			1	1	1	1	1	1	1	1	1		1
S_8	1	1			1	1	1			1	1		1	1	1	1			1	1	1				1	1				1	1				1	1				1

Fig. 5. Switching states sequences in the proposed SVPWM single-phase IS inverter.

The switching states (SS) distribution is shown in Fig. 5. It can be noted that a switching state sequence of sectors III, IV and VII, VIII is the mirror image of sectors I, II and V, VI, respectively. Grey color means conducting semiconductor switches of the inverter. One of the direct criteria of the switching optimization is overall number of transistor commutation per switching cycle. In this case, the overall commutation number per switching cycle is 12. It should be noticed, than in case of dropping modulation index less than 0.5, the sectors II, III, VI and VII will not be involved in the output voltage vector generation. It can be seen from Fig. 3. At the same time, the number of transistor commutation per switching cycle remains the same. It is explained by fact that all sectors have equal commutation number per switching cycle (Fig. 5).

Summarizing above presented approach it includes calculation of the weighting coefficients of the vectors for each sector in order to provide sinusoidal waveform of the output voltage and select a proper switching sequence in order to provide constant voltage across capacitors along with minimum number of transistor switching.

IV. Modified SVPWM for Single-Phase IS-Based Inverter

Incomplete ST states are mentioned in several papers concerning three-phase systems with impedance networks [29], [30]. The feature of this state consists of asymmetrical ST application to one out of two networks. At the same time the voltage applied to the output is not equal to zero. The equivalent circuit of the additional ST state (1,S) for 3L NPC quasi-Z-Source inverter is depicted in Fig. 6. It shows that only the lower part (IS2) of the quasi-Z-Source network corresponds to the ST state. Capacitor C_3 is discharging and C_2 is charging.

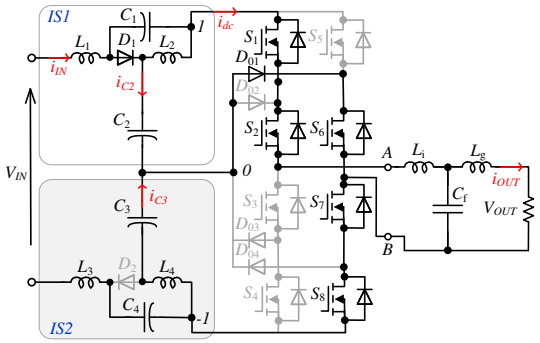
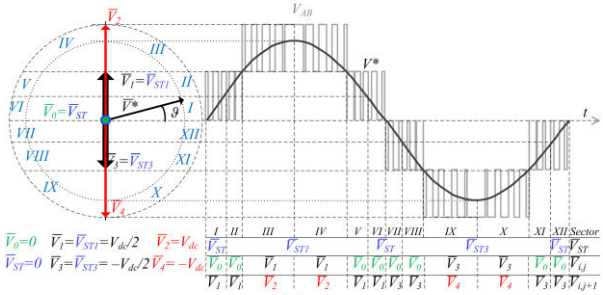


Fig. 6. Equivalent circuit of additional incomplete ST state (1,S) of the quasi-Z-Source NPC inverter.

Additional switching states of incomplete ST can be implemented in order to reduce number of switching. In total, there are four incomplete ST states: (1,S), (S,-1), (S,1) and (-1,S). S denotes an incomplete short circuit when only three switches are opened in the inverter leg. Because of that switching period, both (1,S) and (S,-1) or (S,1) and (-1,S) states should be used during the switching period. Using only one incomplete ST switching state per switching period leads to a capacitor voltage unbalance. However, the voltage V_{AB} at an incomplete ST state is $V_{dc}/2$. These additional states give additional flexibility in the output voltage vector generation. The weighting coefficients and sector boundaries are shown in Table IV.

Fig. 7*a* shows a proposed space vector diagram for the modified SVPWM along with an example of the switching states distribution in each sector.



(a)

Sect.	I					II					III					IV				
Vec.	V_{ST}	V_1	V_0	V_1	V_{ST}	V_{ST1}	V_1	V_0	V_1	V_{ST1}	V_{ST1}	V_1	V_2	V_1	V_{ST1}	V_{ST1}	V_1	V_2	V_1	V_{ST1}
SS	ST	0,-1	0,0	1,0	ST	1,S	1,0	0,0	0,-1	S,-1	S,-1	0,-1	1,-1	1,0	1,S	1,S	1,0	1,-1	0,-1	S,-1
S_1	1			1	1	1	1			1	1			1	1	1	1			1
S_2	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
S_3	1	1	1		1			1	1	1	1	1							1	1
S_4	1				1															
S_5	1				1															
S_6	1		1	1	1	1	1	1						1	1	1	1			
S_7	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
S_8	1	1			1	1				1	1				1	1				1

Sect.	V					VI					VII					VIII				
Vec.	V_{ST1}	V_1	V_0	V_1	V_{ST1}	V_{ST}	V_1	V_0	V_1	V_{ST}	V_{ST}	V_3	V_0	V_3	V_{ST}	V_{ST3}	V_3	V_0	V_3	V_{ST3}
SS	S,-1	0,-1	0,0	1,0	1,S	ST	1,0	0,0	0,-1	ST	ST	-1,0	0,0	0,1	ST	S,1	0,1	0,0	-1,0	-1,S
S_1	1			1	1	1	1			1	1				1					
S_2	1	1	1	1	1	1	1	1	1	1	1	1	1		1	1	1	1		
S_3	1	1	1			1		1	1	1	1	1	1	1	1	1	1	1	1	1
S_4						1				1	1	1			1	1	1			1
S_5						1				1	1				1					
S_6						1				1	1	1			1	1	1			
S_7	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
S_8						1				1	1				1					

Sect.	IX					X					XI					XII				
Vec.	V_{ST3}	V_3	V_4	V_3	V_{ST3}	V_{ST3}	V_3	V_4	V_3	V_{ST3}	V_{ST3}	V_3	V_0	V_3	V_{ST3}	V_{ST}	V_3	V_0	V_3	V_{ST}
SS	-1,S	-1,0	1,-1	0,1	S,1	S,1	0,1	1,-1	-1,0	-1,S	-1,S	-1,0	0,0	0,1	S,1	ST	0,1	0,0	-1,0	ST
S_1																1				1
S_2				1	1	1	1						1	1	1	1		1	1	1
S_3	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
S_4	1	1	1			1	1	1	1	1	1	1			1	1	1			1
S_5	1			1	1	1	1	1	1	1	1			1	1	1			1	1
S_6	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
S_7	1	1				1	1	1			1	1	1			1	1	1		1
S_8																1				1

(b)

Fig. 7. Space voltage vector diagram for proposed modified SVPWM for single-phase 3L NPC IS inverter (a) along with switching states sequences (b).

The switching state sequences for the modified SVPWM are shown in Fig. 7*b*. Vectors V_{ST1} and V_1 are equal and co-directional, as well as V_{ST3} and V_3.

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TABLE IV. WEIGHTING COEFFICIENTS OF MODIFIED SVPWM (FIG. 8)

Weighting coefficients (τ_{ij})	Sector boundaries	
$\begin{cases}\tau_{1,0}=\tau_{6,0}=1-\tau_{ST}-2\cdot V_Y^*\\ \tau_{1,1}=\tau_{6,1}=2\cdot V_Y^*\end{cases}$	$I: 0\le\vartheta<\arcsin\left(\frac{0.5}{M}\right)$	$VI: \pi-\arcsin\left(\frac{0.5}{M}\right)\le\vartheta<\pi$
$\begin{cases}\tau_{2,0}=\tau_{5,0}=1-2\cdot V_Y^*\\ \tau_{2,1}=\tau_{5,1}=2\cdot V_Y^*-\tau_{ST}\end{cases}$	$II: \arcsin\left(\frac{0.5}{M}\right)\le\vartheta<\arcsin\left(\frac{0.5}{M\cdot(1-D_S)}\right)$	$V: \pi-\arcsin\left(\frac{0.5}{M\cdot(1-D_S)}\right)\le\vartheta<\pi-\arcsin\left(\frac{0.5}{M}\right)$
$\begin{cases}\tau_{3,1}=\tau_{4,1}=2-\tau_{ST}-2\cdot V_Y^*\\ \tau_{3,2}=\tau_{4,2}=-1+2\cdot V_Y^*\end{cases}$	$III: \arcsin\left(\frac{0.5}{M\cdot(1-D_S)}\right)\le\vartheta<\frac{\pi}{2}$	$IV: \frac{\pi}{2}\le\vartheta<\pi-\arcsin\left(\frac{0.5}{M\cdot(1-D_S)}\right)$
$\begin{cases}\tau_{7,0}=\tau_{12,0}=1-\tau_{ST}+2\cdot V_Y^*\\ \tau_{7,3}=\tau_{12,3}=-2\cdot V_Y^*\end{cases}$	$VII: \pi\le\vartheta<\pi+\arcsin\left(\frac{0.5}{M}\right)$	$XI: 2\pi-\arcsin\left(\frac{0.5}{M}\right)\le\vartheta<2\pi$
$\begin{cases}\tau_{8,0}=\tau_{11,0}=1+2\cdot V_Y^*\\ \tau_{8,3}=\tau_{11,3}=-2\cdot V_Y^*-\tau_{ST}\end{cases}$	$VIII: \pi+\arcsin\left(\frac{0.5}{M}\right)\le\vartheta<\pi+\arcsin\left(\frac{0.5}{M\cdot(1-D_S)}\right)$	$XI: 2\pi-\arcsin\left(\frac{0.5}{M\cdot(1-D_S)}\right)\le\vartheta<2\pi-\arcsin\left(\frac{0.5}{M}\right)$
$\begin{cases}\tau_{9,3}=\tau_{10,3}=2-\tau_{ST}+2\cdot V_Y^*\\ \tau_{9,4}=\tau_{10,4}=-1-2\cdot V_Y^*\end{cases}$	$IX: \pi+\arcsin\left(\frac{0.5}{M\cdot(1-D_S)}\right)\le\vartheta<\frac{3\pi}{2}$	$X: \frac{3\pi}{2}\le\vartheta<2\pi-\arcsin\left(\frac{0.5}{M\cdot(1-D_S)}\right)$

A switching state sequence of sectors IV-VII and X-XII is the mirror image of sectors I-III and VII-IX, respectively. The overall commutation number per switching period in sectors I, VI, VII, XII is 12. In all other sectors, the overall commutation number is 8. It can be seen that the commutation number in the modified SVPWM (Fig. 7*b*) is significantly reduced compared with SVPWM (Fig. 5). It corresponds to the 22% reduction of overall commutation number in case of $M\cdot=1$.

In advance, the quality of the energy transfer from the source to the load is also improved.

If modulation index is lower, according to the Fig. 7*a*, the involvement of the sectors III, IV, IX and X will be reduced. The modulation index $M\cdot=(1-D_{ST})\cdot 0.5$ is a borderline value when these sectors can be used. Since these sectors have only 8 transistors switching, the overall commutation number will be increased. At the same time, it should be mentioned, that in proper designed inverters, the modulation index lower than 0.5 is not expected. It corresponds to the poor dc-link voltage utilization.

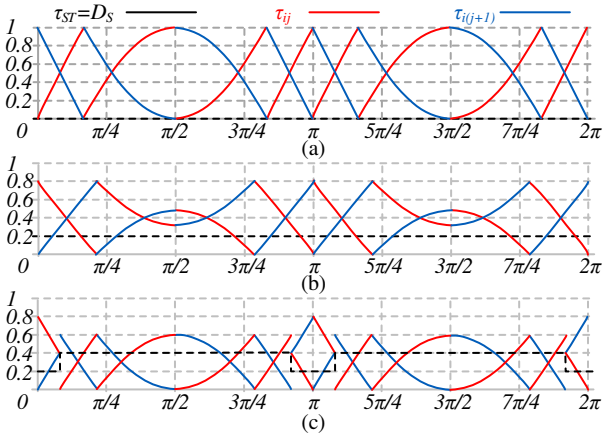

Fig. 8. Graphical representation of the weighting coefficients of: (a) both SVPWM, M=1, D_{ST}=0; (b) the SVPWM, M=1, D_{ST}=0.2; (c) the modified SVPWM, M=1, D_{ST}=0.2.

Finally, in graphical representation of the weighting coefficients is shown in Fig. 8. Fig. 8b and Fig. 8c illustrates the weighting coefficients for the case with ST duty cycle which is equal D_{ST}=0.2 and modulation index M=1 correspondently. From Fig. 3, 7 and Table III, IV it can be seen that boundaries of the sectors strictly depends on the amplitude of ST duty cycle. However if M=1 and D_{ST}=0 both SVPWMs have equal weighted coefficients representation like in Fig. 8a.

V. SIMULATION AND EXPERIMENTAL VERIFICATION

In order to verify the proposed approaches and to demonstrate the feasibility of the practical implementation, a comprehensive simulation and experimental study was performed. The main goal was to compare the proposed SVPWM for single-phase IS networks with existing modulation techniques. The value of components and parameters of the chosen topology are presented in Table IV [15], [16].

TABLE IV. COMPONENTS AND PARAMETERS OF 3L NPC QUASI-Z-SOURCE INVERTER USED FOR EXPERIMENTS

Input dc voltage V_{IN}	240-450 V
Output ac RMS voltage V_{OUT}	230 V
Nominal output power	1 kW
Capacitance value of the capacitors C_1 and C_4	1 mF
Capacitance value of the capacitors C_2 and C_3	0.4 mF
Inductance value of the inductors L_1... L_4	240 µH
Inverter side inductor filter L_I	0.44 mH
Output side inductor filter L_g	0.2 mH
Capacitor filter C_f	0.47 µF
Switching frequency f	120 - 240kHz
Control Unit (FPGA)	Cyclone IV EP4CE6E22C8
Control Unit (MC)	STM32F417ZET
Transistors Driver Chip	ACPL-H312
Transistors S_1... S_8	IPW65R041CFD
quasi-Z-Source and NPC diodes D_1... D_6	C3D10065A SiC Shottky

Fig. 9 shows the experimental setup. It consists of the inverter PCB board, a quasi-Z-Source board with external quasi-Z-Source inductors and output filters. The values of the passive components are shown in Table IV. Also, the control board is shown in Fig. 9. Table IV shows the values of passive elements along with types of selected semiconductors. It should be underlined that conventional Si MOSFET transistors from Infinion are selected. They belong to the family with very fast body diode and are adopted for inverter application. At the same time SiC diodes are selected as clamping diodes and diodes for

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quasi-Z-source network. Any other types of diodes are not suitable for high switching frequency in IS based converters.

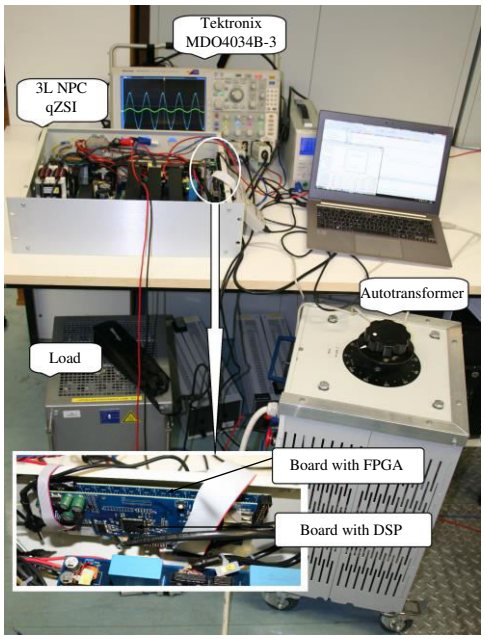

Fig. 9. Photo of the experimental setup along with the control board.

All the measurements were made by the digital oscilloscope Tektronix MDO4034B-3, current probes Tektronix TCP0150, and voltage probes Tektronix TPA-BNC. Fig. 9 shows a zoomed picture of the control board. It was specially designed for this application. The control system consists of two boards based on a combination of the low cost Field-Programmable Gate Array (FPGA) and Microcontroller (MC) with Floating-point Unit (FPU). The bottom side board has a low cost FPGA from Altera Cyclone IV EP4CE6E22C8. The upper side board has MC STM32F417ZET correspondingly. Each of these parts can work independently and communicate through Serial Peripheral Interface (SPI). Such combination provides an effective performance of any complex control.

Fig. 10 shows the diagram of the calculation sequence of the SVPWM techniques. First of all it can be seen that calculation is distributed between MC and FPGA. The reference sinusoidal voltage V_{REF} is the input signal for MC. This signal is derived from another block that is not topic of discussion of this paper. The ST duty cycle D_S is derived from other control unit as well.

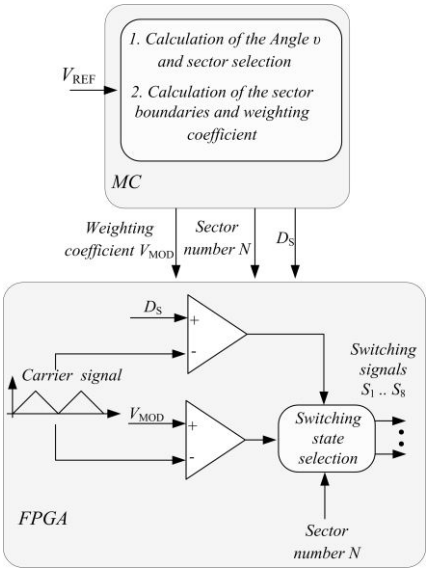

Fig. 10. Diagram of the calculation sequence of the SVPWM.

According to the phase and amplitude of the reference sinusoidal voltage MC defines the sector number along with weighting coefficient of the vectors. The FPGA is a suitable tool to realize a very high PWM switching frequency. The switching state selection that is realized in the FPGA requires no powerful computing resources. FPGA based on received weighting coefficient and sector number defines the switching states of transistors. It should be noted that final switching frequency can be much higher than frequency of data exchange between MC and FPGA. The switching frequency is defined by carrier signal in FPGA.

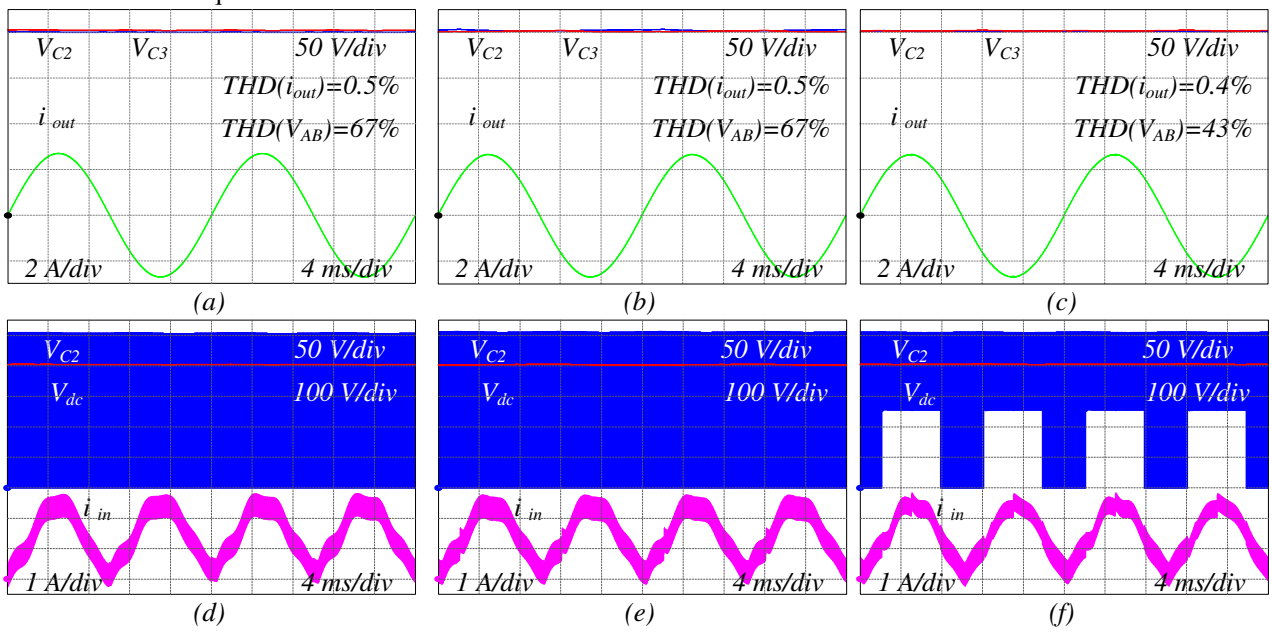

Fig. 11.Simulation results of SPWM (a), (d) proposed SVPWM modulation technique (b), (e) and modified SVPWM (c), (f).

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As a result, the control system described above can provide the proposed SVPWM with very high switching frequency and good resolution. At the same time, this control board contains a low cost FPGA and MC that makes it economically viable. In this particular case the switching frequency was reconfigured from 120 kHz till 240 kHz while data exchange frequency was constant 15 kHz.

The modulation technique described above [49] was selected as a reference for our comparison. Fig. 11 shows the simulation waveforms. The input voltage is equal to 300 V with D_S=0.2, output power is about 400 W. The average voltage across capacitors is 400V while the RMS value of output voltage is 230 V. It corresponds to the modulation index M=0.8. Simple resistor is used as a load. Fig. 11*a,d* illustrate the simulation results with the reference SPWM. At the same time, Fig. 11*b,f* show the results demonstrated with the proposed SVPWM. Finally, Fig. 11*c,g* show the proposed modified SVPWM. The dc-link voltage shape V_{dc} of the modified SVPWM differs from other modulations. Incomplete ST states correspond to the half of dc-link voltage.

It can be seen that, all the methods provide a stable voltage across the capacitors and Total Harmonic Distortion (THD) of the output current is very close. At the same time in case of modified SVPWM technique the THD of the output voltage before filter is lower which in turns provides lower THD of the output current. Modified solution has 43% compare to 67% in SVPWM and PWM approaches. It is explained by reduced amount of zero states in dc-ink voltage.

Fig. 12 shows experimental results for SPWM and both SVPWM techniques for fundamental cycle. It shows the dc-link voltage waveform, capacitor voltage along with input current waveforms. First of all this figure shows ability to work at very high switching frequency (240 kHz). Peak value of the input current is about 3 A, average value twice lower. Despite the very high switching frequency noise presence it can be seen that experimental results are in good correspondence with the simulation results. In case of modified SVPWM (Fig. 12c) the dc-link voltage is different due to the presence of incomplete ST states.

Fig. 13 shows experimental results for only modified SVPWM technique for fundamental (Fig. 13*a*) and switching cycles (Fig. 13*b* and Fig. 13*c*) with the same load condition (400 W). The output current along with capacitor voltage is shown in Fig. 13*a*. It shows that output current waveform is sinusoidal and is with good agreement with simulation results. Incomplete ST states are utilized and provides transient between neighbor states with minimum transistor switching. Fig. 13*b* shows the switching cycle when incomplete and full ST states are implemented, while only incomplete ST states generation is demonstrated in Fig. 13*c*. The input current for switching cycles is demonstrated as well. Because of very high switching frequency the ripple of the input current is very small.

To demonstrate difference between techniques, the number of switching transients (times) in one switching cycle (defined at 50 Hz) was analyzed. These numbers are related to the switching losses represented in Fig. 14 for each modulation technique (D_s is larger than 0). From [49] it is clear that to provide the same ST switching frequency, the carrier signal of the proposed SVPWMs must have the double switching frequency.

Even at double frequency, in the proposed modified SVPWM, the switching states are much more reduced than in the special carrier-based SPWM. At the same time, the overall switching numbers in the proposed SVPWM are approximately the same as in the special carrier-based PWM. The advantage of the SVPWM over the SPWM is in the switching stress between the transistors that are more equally distributed.

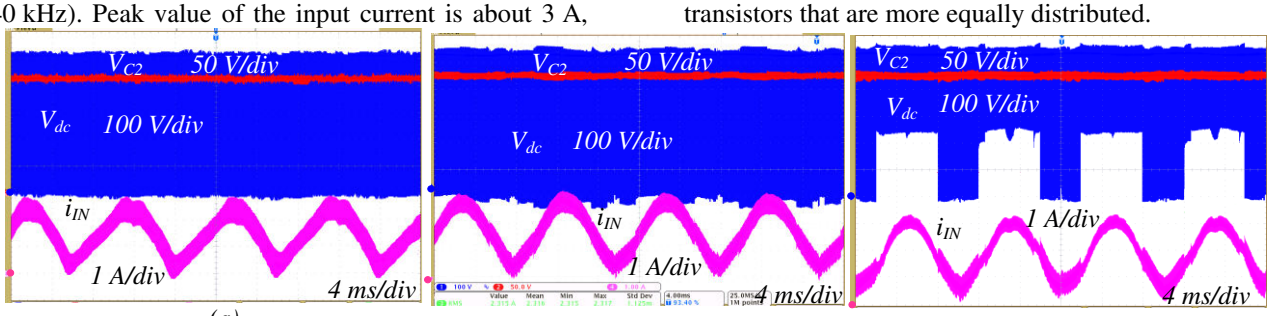

Fig. 12.Experimental results with dc-link voltage, capacitor voltage and input current: SPWM (a), SVPWM (b and modified SVPWM (c).

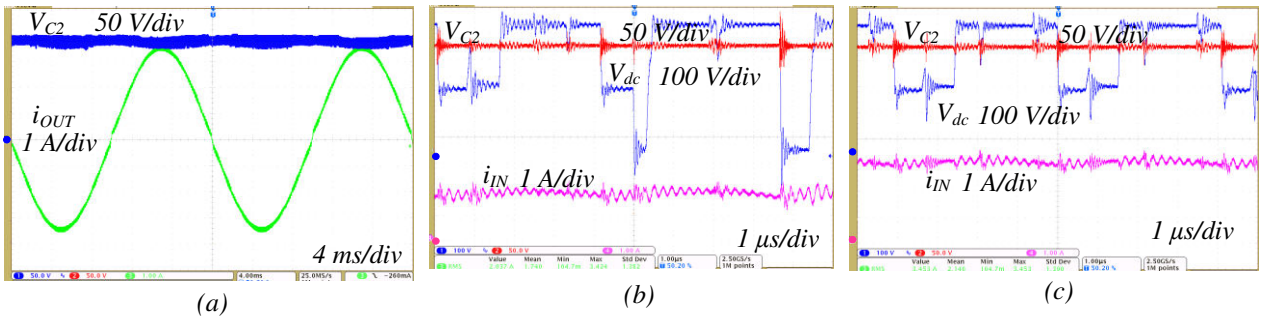

Fig. 13.Experimental results of modified SVPWM: fundamental cycle (a), switching cycle (b) and (c).

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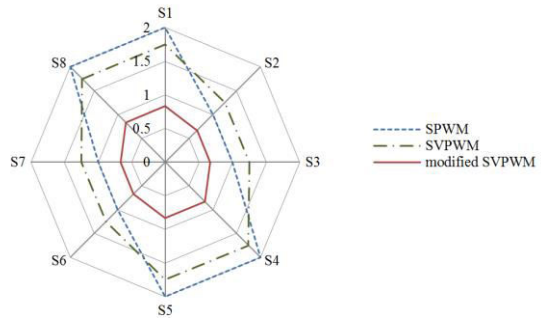

Fig. 14. Number of switching transients in one switching cycle. SPWM modulation technique versus the proposed SVPWM techniques.

In conclusion, it can be predicted that the modified SVPWM will have lower switching losses. In order to verify this prediction, several tests with different switching frequencies and level of power are performed. Fig. 15a shows the efficiency dependence versus the switching frequency while Fig. 15b shows the efficiency dependence versus the output power with the same input voltage (300 V) and constant ST duty cycle D_s=0.2.

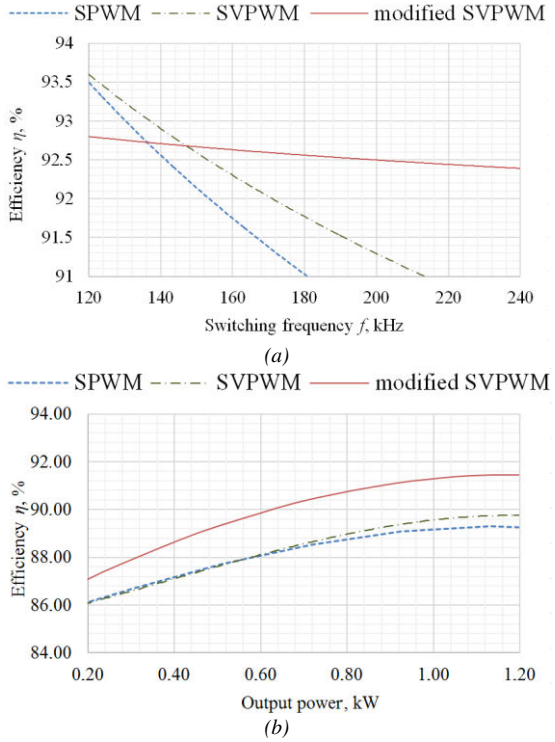

Fig. 15.Experimental efficiency versus switching frequency for the different SVPWM techniques for a single-phase IS inverter (a) and efficiency versus output power with switching frequency 240 kHz (b).

It can be seen that the efficiency in the case of the SPWM is significantly reduced by increasing the switching frequency. A similar effect can be observed for the SVPWM and the modified SVPWM. At the same time, it can be seen that the level of incline is different. It means that the level of switching losses in the case of both SVPWMs is lower, in particular in the case of the modified solution. Also, it is evident that in the modified SVPWM, conduction losses are higher. As a result, the overall efficiency is lower at relatively low switching frequency, and significantly better at high switching frequency. Similar effect can be observed with power increasing. There is some optimal point with the best efficiency, further power increasing will lead to efficiency decreasing.

VI. Conclusions

This paper has presented novel SVPWM strategies for the single-phase 3L buck-boost full-bridge NPC inverter coupled with IS network. The proposed approach has a minimum number of switching and, as a result, the improved performance is demonstrated in terms of switching losses reduction. The output voltage quality is not worse compared with the traditional PWM strategies. Finally, the switching losses are equally distributed among transistors. Also, the proposed solutions have balanced utilization of all capacitors of the IS network which remains voltage across capacitors stable.

It should be noticed, that as any SVM technique, more complex calculation compare to the PWM is required. The main drawback of the proposed technique consists in the increased conduction losses due to the utilizing only single leg of the full-bridge NPC converter during ST generation. It belongs mostly to the MOSFET transistors, where losses are proportional to the drain-source resistance. Because of that, such approach can be recommended for inverters realized by MOSFET transistor with very high switching frequency, where switching losses dominates over conduction losses. Another application can be based on IGBT transistors, where switching losses decreasing will allow increasing switching frequency.

Theoretical claims are verified by means of simulation and experimental study.

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